Process and Packaging Innovations for Moore’s Law Continuation and Beyond   
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***Abstract*—** This presentation describes various revolutionary process and packaging technologies on the horizon that will (i) extend Moore’s Law scaling through and beyond the next decade and (ii) enable many new, exciting integrated circuit opportunities and functions for future products. By using these new and exciting technologies holistically, and coupled with technology and design co-optimization, the future of Moore’s Law is brighter than ever.

**I.INTRODUCTION**

For the last 50 years Moore’s Law has been the guiding principle for the silicon industry, enabled by numerous process innovations. Yet in the last few years there has been great concern that Moore’s Law will soon come to a halt. This presentation will describe various revolutionary process and packaging technologies on the horizon that will enable both monolithic and system 3D heterogeneous integration to

scaling, as shown in Figure 1, thereby providing a viable path for density scaling and Moore’s Law continuation through and beyond the next decade.

**III.MONOLITHIC 3DHETEROGENEOUS**  **INTEGRATION**

The capability of monolithic heterogeneous integration offers many attractive enabling technology options such as (i) Ge PMOS/Si NMOS for high-performance low-power CMOS and (ii) GaN NMOS/Si CMOS for energy-efficient, compact 5G and power delivery. Such capabilities will not be enabled by direct materials growth alone due to large lattice mismatches, but rather by the advancement of both epitaxy and 3D layer transfer technologies. A Ge PMOS transistor with the best-ever reported ION-IOFF performance achieved using 300mm 3D layer transfer technology, as shown in Figures 2-4, will be reported in this IEDM conference by W. Rachmady [2]. In

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| --- | --- | --- | --- | --- | --- | --- |
| continue | Moore’s | Law | scaling, | while | improving | addition, industry’s first 300mm 3D heterogeneous integration |

performance/Watt. Beyond EUV capability, new patterning techniques using DSA [1], new interconnects using subtractive metal etch and 2D barriers, high performance Ge [2] and 2D-material transistors [3,4], high-mobility wide-bandgap GaN

of enhancement-mode GaN NMOS and Si PMOS transistors on 300mm high resistivity Si(111) substrate, achieved using GaN MOCVD epitaxy and 3D layer transfer technology, as shown in Figures 5-6, will be reported in this conference by H.W. Then

devices [5], hybrid bonding [6,7] and Omni Directional [9].

Interconnect for packaging [8], are all viable enablers. Furthermore, many of these new technologies enable new, exciting integrated circuit opportunities such as monolithic co-integration of GaN devices and Si CMOS on the same wafer for future 5G and power delivery products [9]. By using these new and exciting technologies holistically, and coupled with technology and design co-optimization, the future of Moore’s Law is brighter than ever.

**II.TRANSISTOR SCALING**

Over the last two decades transistor scaling and performance have been enabled by innovations such as strained-Si channel, high-K/metal-gate [10], FinFET [11] and self-aligned contacts. FinFET, in particular, improves electrostatics over planar transistors and enables continued LG scaling. However for further LG scaling and hence, gate pitch scaling beyond what the FinFET can provide, gate-all-around (GAA) transistors such as nanowires and nanoribbons [12,13] will need to be employed. Transistors with 2D channel materials such as MoS2, WS2 and WSe2 will also be considered as they offer the best electrostatics and most LG scaling [4]. Both GAA devices and 2D-material transistors will require multiple channels for high drive current. In addition to gate pitch scaling, monolithic 3D transistors stacking can be employed to enable cell height scaling. Coupling GAA devices or 2D-material transistors with monolithic 3D transistors stacking enables both gate pitch and cell height

**IV.INTERCONNECT**

Interconnect plays a critical role in Moore’s Law and looking ahead new, revolutionary process technologies will be needed to enable continued Cu interconnect scaling and performance. Three novel technologies have the potential to bring about disruptive benefits: (i) subtractive metal process, (ii) ultra-thin 2D-material barriers, and (iii) selective via fill, as shown in Figure 7. Subtractive interconnect technology and/or ultra-thin 2D-material barrier technology using TMD or graphene will be needed to address the thickness scaling limit of current Cubarriers (e.g. Ta, TaN) which is ~2.5nm, in order to enable sub-30nm metal pitch scaling with high performance especially for the lower interconnect layers. For the middle Cu interconnect layers with 40-60nm pitch, the interconnect R-C performance is enhanced with increasing aspect ratio (AR), defined as total (trench + via) height post polish divided by the trench width, as shown in Figure 8. A robust selective via fill process (e.g. Ru, Co) followed by Cu fill will be employed to enable high-AR gap-fill for improved R-C performance. Moreover, significant additional improvement in capacitance can be achieved with the use of airgaps, as shown in Figure 8-9.

**V.DIRECTED SELF ASSEMBLY (DSA)PATTERNING**

As feature sizes continue to shrink for density scaling, the ability to print and to correctly place tight-pitch patterns are

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vital for Moore’s Law continuation. While the print capability is being addressed by spacer-based pitch division and EUV, these patterning techniques will not address shortcomings in edge placement error (EPE) especially for tight pitches below 30nm, due to the fundamental physical limitations of conventional optical lithography. Looking ahead a new DSA patterning technology (Figure 10) which combines (i) forming chemical patterns with looser pitch using conventional optical lithography and (ii) using those as guide patterns for the self-assembly of block co-polymers (BCPs) to form new line space patterns with >3X denser pitch than the chemical guide patterns [1], will need to be employed to enable sub-30nm pitch scaling with much improved EPE performance. Figure 11 shows that the spacing variation in 30nm-pitch line-space patterns is significantly improved with the use of DSA

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| patterning | compared | to | spacer-based | pitch | division. |

Furthermore, DSA-defined pitch down to 22nm has been demonstrated, as shown in Figure 12.

**VI.SYSTEM 3DHETEROGENEOUS INTEGRATION**  **AND PACKAGING**

System 3D heterogeneous integration which drives towards achieving a large System-in-Package (SiP) composed

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| of | different | process-optimized | chiplets | with | overall |

performance approaching that of monolithic integration, as

the best energy-delay characteristics amongst all the beyond CMOS devices studied, as shown in Figure 16. The fabrication and device characteristics of the MESO device will be reported by C.-C. Lin in this conference [15].

**VIII.DENSE MEMORY-LOGIC INTEGRATION**

Dense memory-logic integration for future compute-near-memory and AI applications is an important vector in driving Moore’s Law continuation and beyond, which can be enabled by system 3D heterogeneous integration using hybrid bonding and ODI. With the advancement of layer transfer technology and memory material deposition technologies, multi-layer/stackable memory elements on Si CMOS via 3D heterogeneous integration, as shown in Figure 17, can be made into a viable option. A low-voltage single-transistor memory element made using stackable materials and low-temperature processing, as shown in Figure 18, will be an attractive candidate for such a scheme. Furthermore, the emergence of Spin Orbit Torque (SOT)-MRAM [21] which has potentially higher density with speed approaching that of 6T-SRAM, can be used for future last level cache applications using monolithic integration scheme, as shown in Figure 19.

**IX.CONCLUSION**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| shown in Figure 13, is another exciting and vital approach | Numerous | revolutionary | process | and | packaging |

besides monolithic 3D integration for enabling Moore’s Law continuation and new product opportunities. A key focus for this approach is to ensure that the in-package connectivity can both perform with low overhead and support similar bandwidth and connection densities as on-die interconnects. This can be made possible by using the hybrid bonding technology [6,7] to replace the conventional solder bond technology to significantly increase the vertical density of connections/area for die-to-wafer and/or wafer-to-wafer stacking. Another novel approach is Omni-Directional Interconnect (ODI), as shown in Figure 14, which allows (i) a high bandwidth fine pitch connection of top die to base die, (ii) a bottom die to package connection for power and IO, and (iii) a new direct connection of top die to package that supports direct power delivery comparable to monolithic implementations. ODI packaging provides new degrees of freedom in 3D die stacking for system 3D heterogeneous integration which result in multiple performance benefits including lower latency, lower energy per bit and higher bandwidth density. The ODI technology will be reported by A. Elsherbini in this IEDM conference [8].

**VII.BEYOND-CMOS**

Scaling of CMOS electronics according to Moore’s Law faces challenges not only from the ability to pattern smaller devices, but also from the level of power dissipation on chip. One important forward-looking device research vector is to identify an energy-efficient switch beyond CMOS for future energy-efficient logic and integrated circuits. The methodology of benchmarking of beyond CMOS devices [14] resulted in the identification of the magnetoelectric spin-orbit (MESO) logic device (Figure 15) as the most promising device candidate with

innovations are on the horizon for enabling Moore’s Law scaling and performance through and beyond the next decade, and for enabling many new and exciting integrated circuit opportunities and functions. By using these new and exciting technologies holistically, and coupled with technology and design co-optimization, the future of Moore’s Law is brighter than ever.

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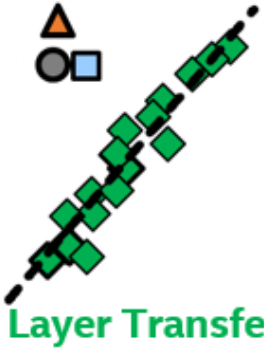
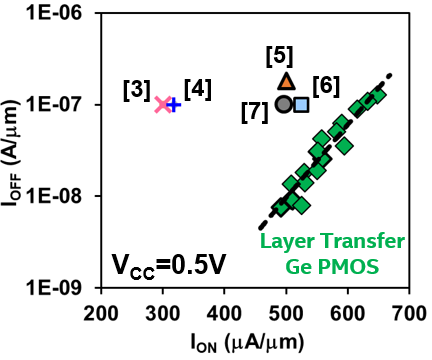
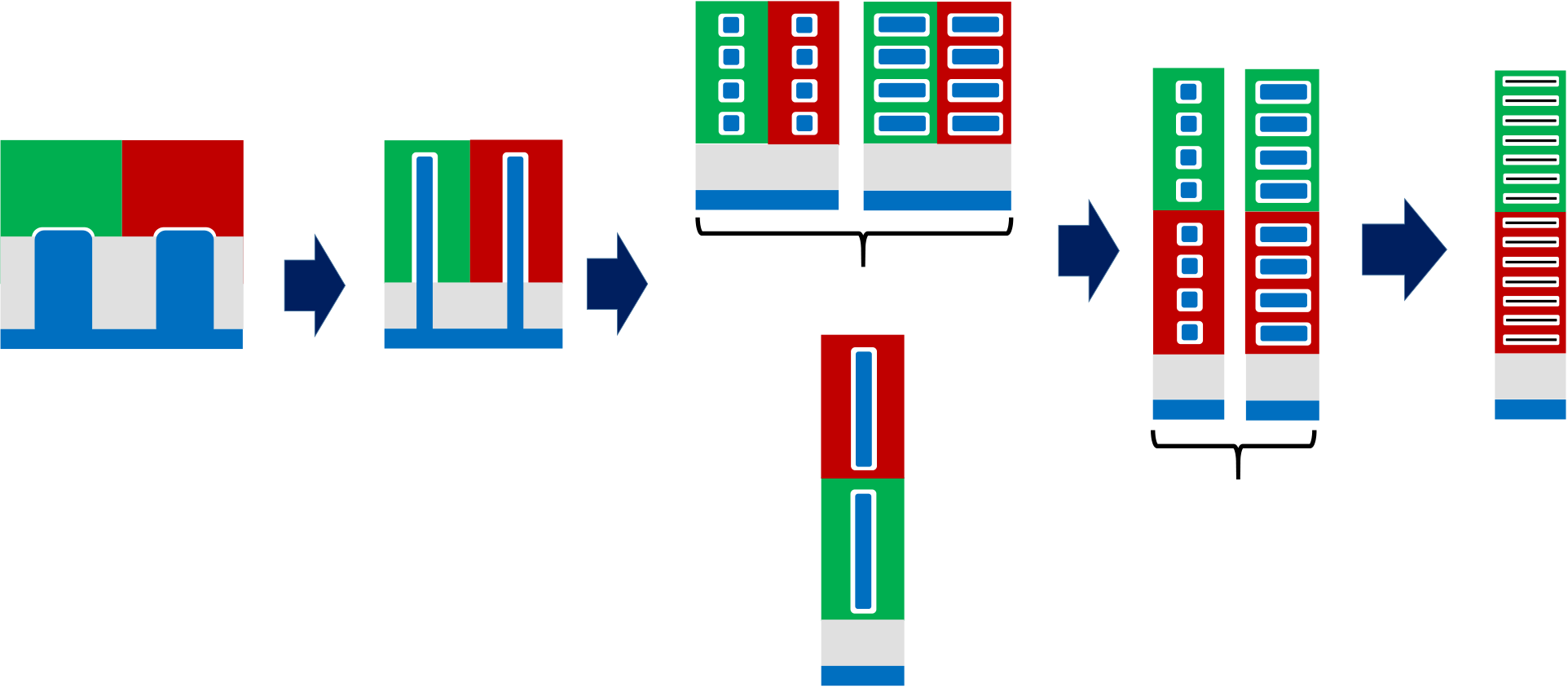
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**Gate**   
**Pitch**   
**Scaling**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **NMOS** | **PMOS** | **Gate** | **FinFET** | **Cell** | **Gate** | **Stacked**  **2D-Material Transistors** |
| **Height** | **Pitch** |
| **Pitch** | **Scaling** | **Scaling** |
| **Gate** | **Gate** | **Scaling** | **Nanowire or Nanoribbon** | |
| **Isolation**   **Si**  **Substrate** | |
| **Planar** | | **Cell** | |
| **Height** | |
| **Scaling** | |
| **Nanowire or Nanoribbon** | |
| **3D Stacking** | |

**FinFET**   
**3D Stacking**

Fig. 1. Transistor structures and architectures for Moore’s Law continuation.

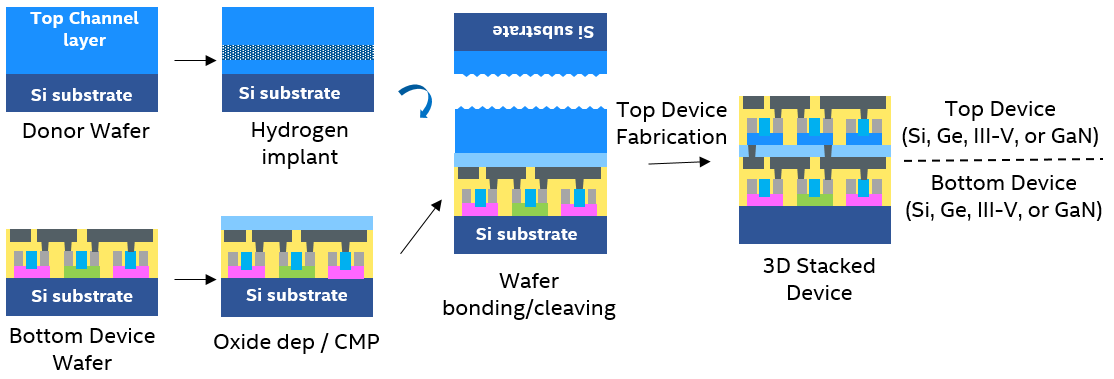
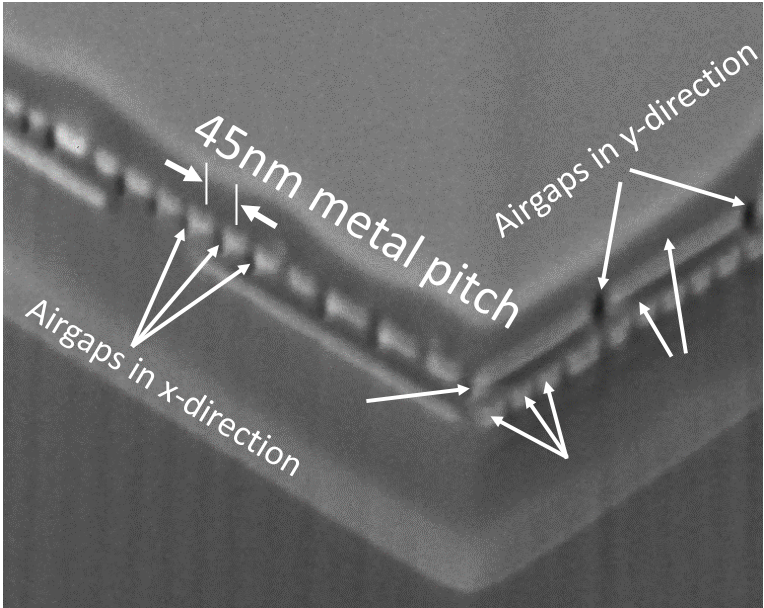
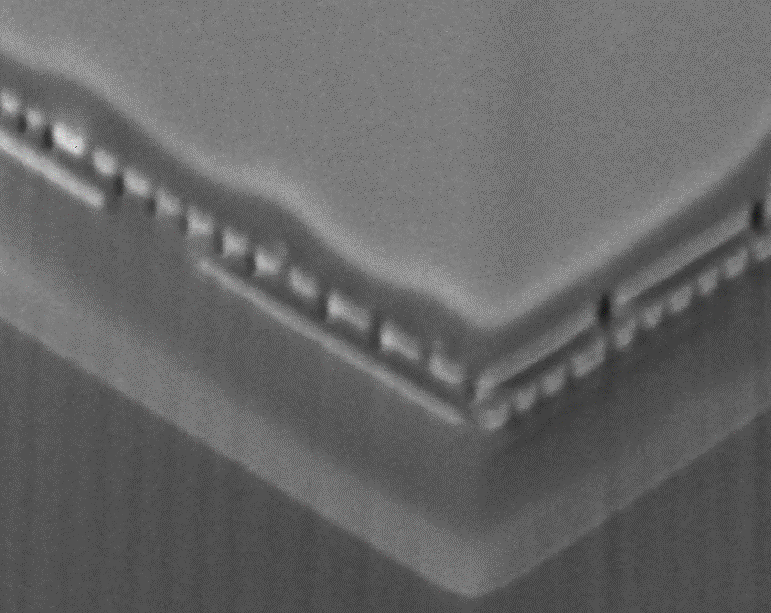
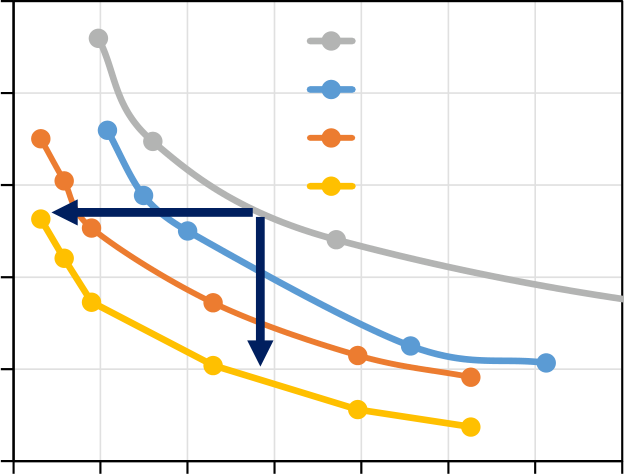
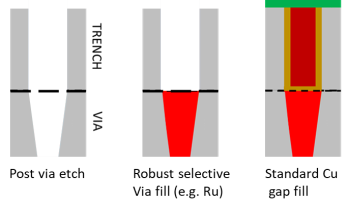
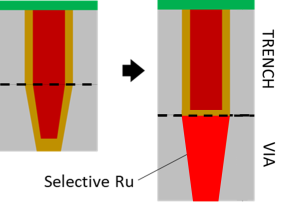
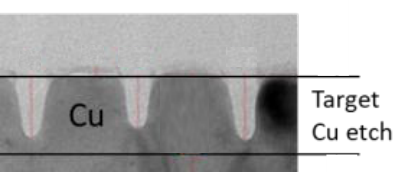
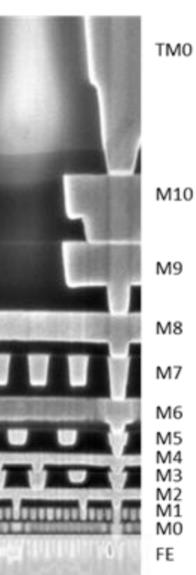
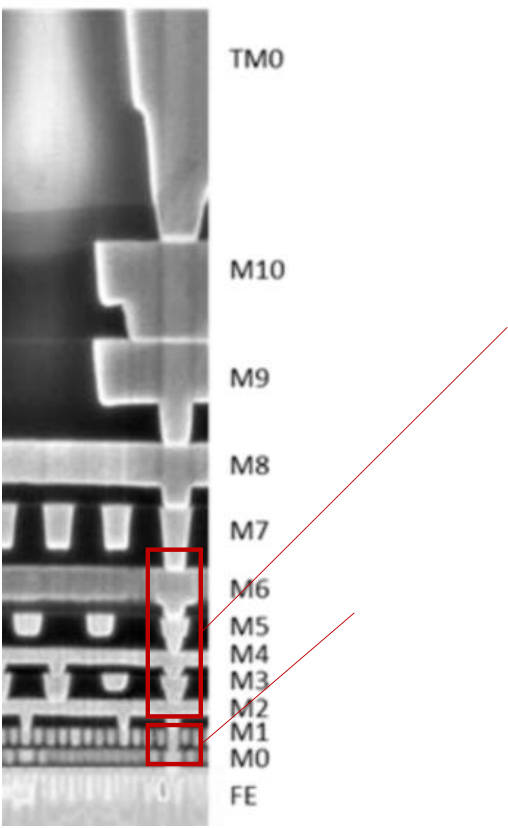
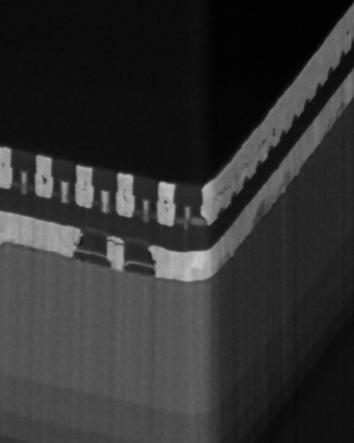
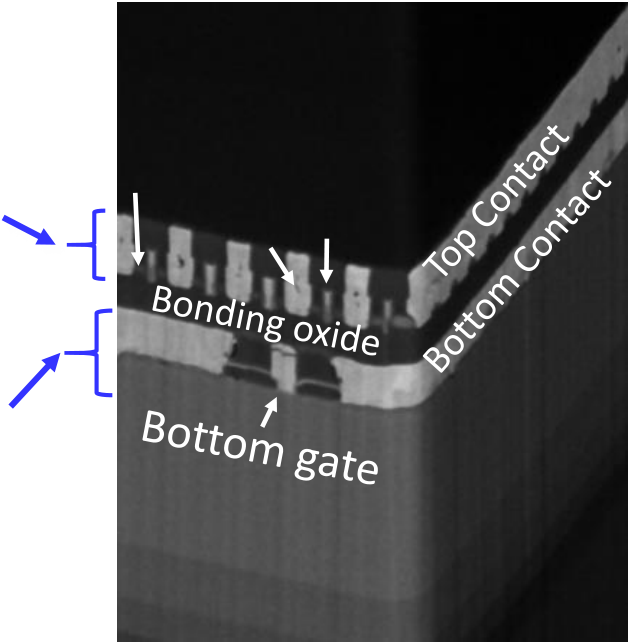
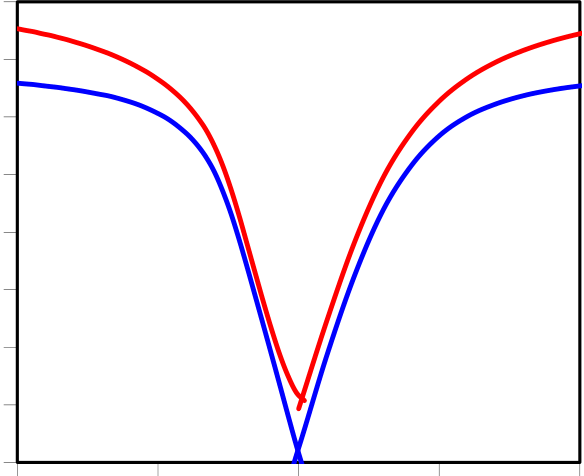


Fig. 2. Monolithic 3D heterogeneous integration using layer transfer technology [W. Rachmady (Intel), this IEDM; H.W. Then (Intel), this IEDM].

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Fig. 3. Monolithic 3D stacked Ge PMOS on Si NMOS using 300mm layer transfer technology [W. Rachmady (Intel), this IEDM]. | **[18]** | | | | | | | |
| **[16]** | | | **[17]** | | **[20]** | **[19]** | |
| Fig. 4. Ge PMOS transistor using 300mm 3D layer transfer | | | | | | | |
| technology | shows | | the | best-ever | | reported | ION-IOFF |
| performance to-date [W. Rachmady (Intel), this IEDM]. | | | | | | | |
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**(b)**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Si Transistor** | Top Epi S/D | Top contact | Top Gate | **ID (A/**m**m)** | **1.0E-03 1.0E-04** | **VD=-1.2V** | | **0** | **VD=1.2V** | |
| **(top device layer)** | **1.0E-05** | | | **VD=50mV** | |
| **1.0E-06** | **VD=-50mV** | |
| **GaN Transistor** | **1.0E-07** | | | **GaN NMOS** | |
| **1.0E-08** | | |
| **1.0E-09 1.0E-10 1.0E-11** | **Si PMOS**  **LGp=130nm** | |
| **(bottom** |
| **LGn=180nm** | |
| **device layer)** |
| **0.6** | **1.2** |
| **-1.2** | | **-0.6** |

Fig. 5 Industry’s first 300mm 3D heterogeneous integration of GaN NMOS and Si PMOS transistors on 300mm high resistivity Si(111) substrate achieved using GaN MOCVD epitaxy and 3D layer transfer technology. [H.W. Then (Intel), this IEDM]

**SELECTIVE VIA**

**FILL FOR**

**VG (V)**   
Fig. 6 shows ID-VG characteristics of the top Si PMOS

transistor and the bottom GaN NMOS transistors.

[H.W. Then (Intel), this IEDM]

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  | **HIGH AR > 4.0** | **Selective Via fill** | **Post Via etch** | **Selective Via fill** | **Standard** |
| **Improve** |  |  |  |  |  | **Cu gap fill** |

**40-60 nm Metal Pitch**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **C. Auth et al, IEDM (2017)** | **Performance** | |  |  |
| **2D-MATERIAL BARRIER** | |
| **Enable** |  |
| **<30 nm Metal Pitch** | |  | Cu |
| **Scaling and Performance** | |
|  | |
| **SUBTRACTIVE Cu** | |

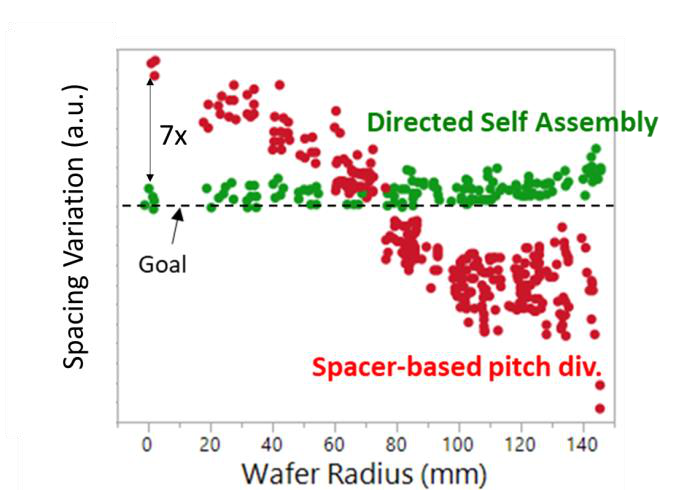
Fig. 7 shows three novel interconnect technologies which have the potential to bring about disruptive benefits: (i) subtractive metal process, (ii) ultra-thin 2D-material barriers, and (iii) selective via fill.

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Capacitance (normalized)** | **1.5** | **0.6** | **AR = 2** | | | | | | **2.0** | via | ILD |
| **1.3** | **AR = 3** | | | | | |
| **AR = 4** | | | | | |
| **1.1** |
| **AR = 4 + Airgap** | | | | | |
| **0.9** |
| **0.7** |
| **0.5** | **0.8** | **1.0** | **1.2** | **1.4** | **1.6** | **1.8** | Metal |
| **Resistance (normalized)** | | | | | | Interconnect |

Fig. 8 shows the interconnect R-C performance improves with increasing aspect ratio (AR), defined as total (trench + via) height post polish divided by the trench width.

Fig. 9 shows the SEM cross-section of the 45nm-pitch metal interconnect with airgaps.

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|  |  |  |
| --- | --- | --- |
| |  | | --- | |  | | **7x**  **30nm Pitch** |

Fig. 10 shows the DSA patterning technology which combines (i) forming chemical patterns with looser pitch using conventional optical lithography and (ii) using those as guide patterns for the self-assembly of block co-polymers (BCPs) to form new line space patterns with >3X denser pitch than the chemical guide patterns [1].

Fig. 11 shows the spacing variation in 30nm-pitch line-space patterns is significantly improved with the use of DSA patterning compared to spacer-based pitch division.

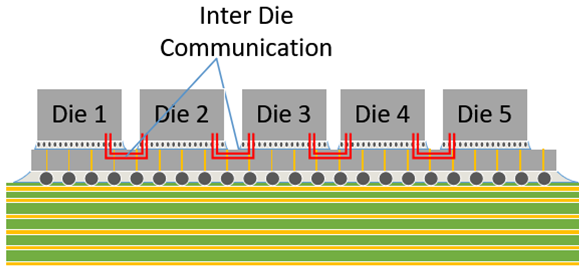


Fig. 13 shows system 3D heterogeneous integration resulting in a large System-in-Package (SiP) composed of different process-optimized chiplets with overall performance approaching that of monolithic integration.

Fig. 12 shows DSA-defined pitch of 22nm has been   
demonstrated.

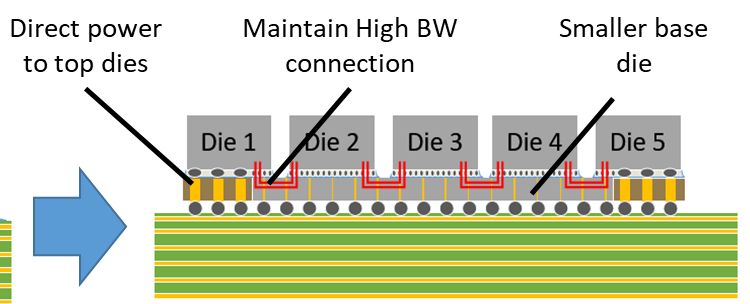


Fig. 14 shows the Omni-Directional Interconnect (ODI) which provides a new degree of freedom in 3D die stacking and multiple performance benefits including lower latency, lower energy per bit and higher bandwidth density. [A. Elsherbini (Intel), this IEDM]

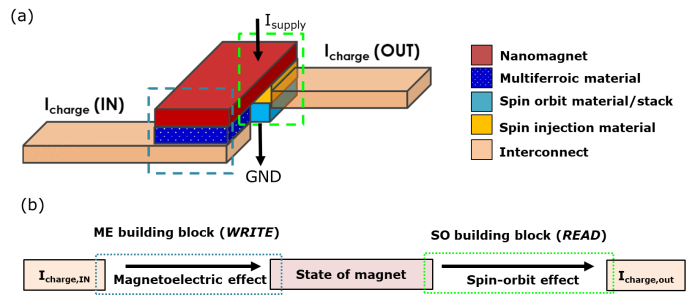


Fig. 15 (a) Schematic structure of the magnetoelectric spin orbit (MESO) logic device. (b) Path of transduction of logic state in one MESO logic gate. Charge currents in the interconnect between devices carry this logic information to the next stage of MESO gates. [C-C.Lin (Intel), this IEDM]

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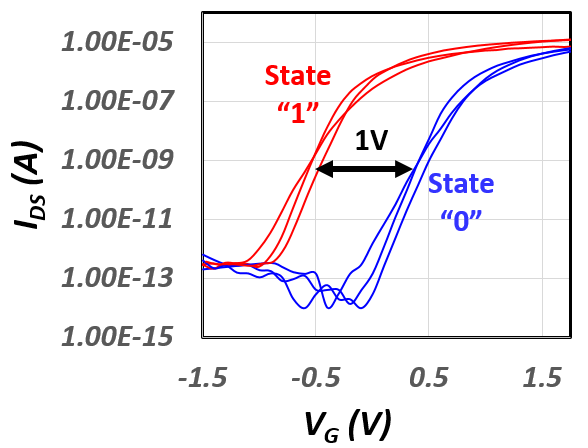
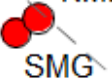
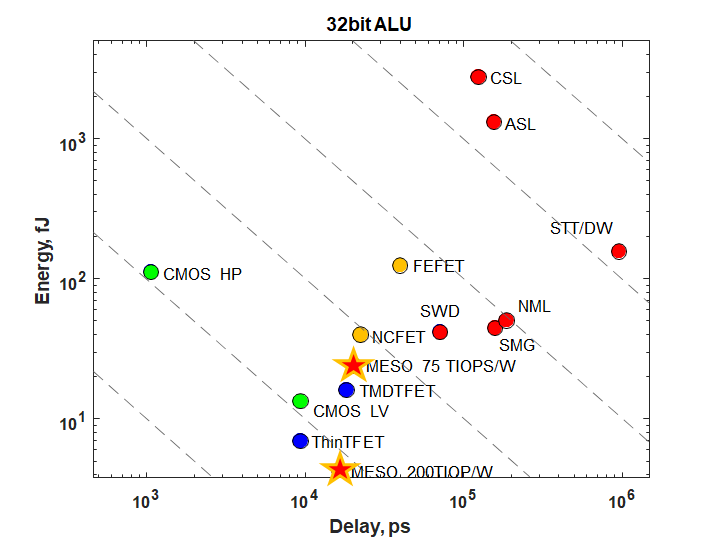
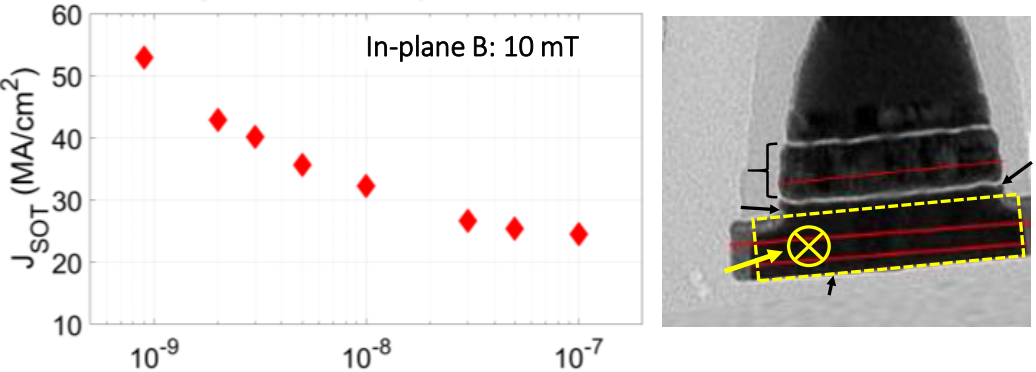
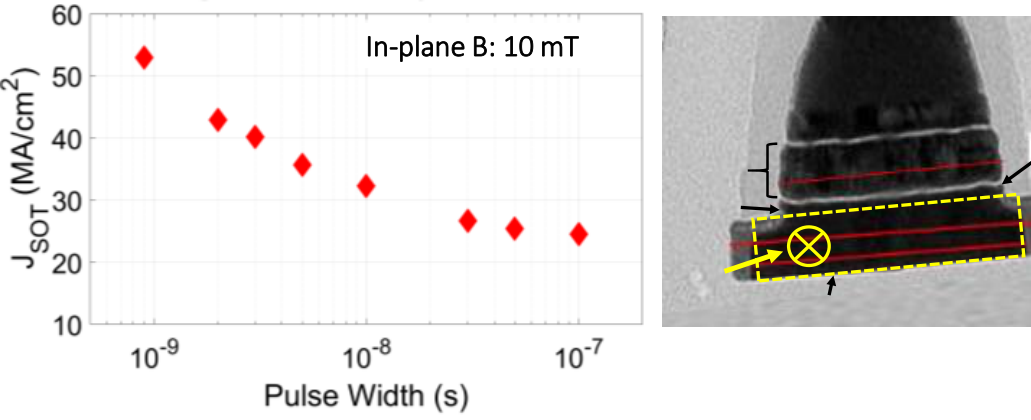
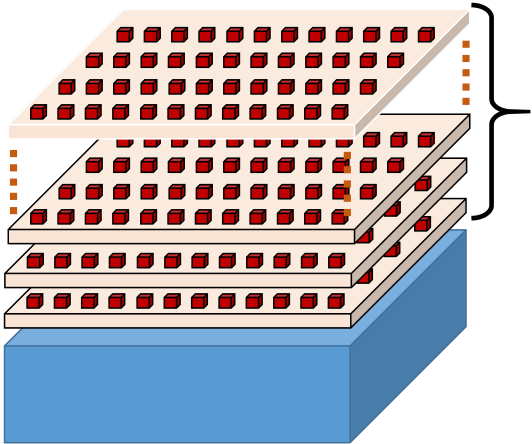


Fig. 16 Energy vs. Delay of 32-bit ALU operation for CMOS and beyond-CMOS devices. STT-DW, spin-transfer-torque domain-wall device; ASL, all-spin-logic device; CSL, charge spin logic; NML, nanomagnetic logic; SMG, spin majority gate; SWD, spin wave device; CMOS HP, high-performance CMOS at 0.73 V supply; CMOS LV, low-power CMOS operating at 0.3 V supply; FEFET, ferroelectric FET; Thin TFET, 2D-material vertical tunnel FET; TMDTFET, transition-metal dichalcogenide tunnel FET; MESO, magnetoelectric spin-orbit device [14].

**Multi-layer**

**Low-temperature process**

**Monolithic**

**High-Density Memory**

**Si CMOS Logic**

Figure 17 shows the multi-layer/stackable memory elements   
on Si CMOS via 3D heterogeneous integration.

|  |  |  |
| --- | --- | --- |
| In-plane B: 10 mT | **Ta/Ru** | Figure 18 shows the measured IDS-VG of a FeFET single |
| transistor memory after applying programming voltage |

of +1.7V and erase voltage of -1.5V at VDS=0.1V,

|  |  |  |
| --- | --- | --- |
| **SAF/** | **MgO** | demonstrating a memory window of 1V. |
| **Fixed Layer** |

**Free Layer**

**JSOT**

**SOT Electrode (W/Ta)**

Figure 19 shows SOT switching current density versus switching pulse width demonstrating SOT-MRAM can be operated down to 0.9 ns with a switching voltage of 0.19V. The device has scaled SOT electrode width of 100nm.

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